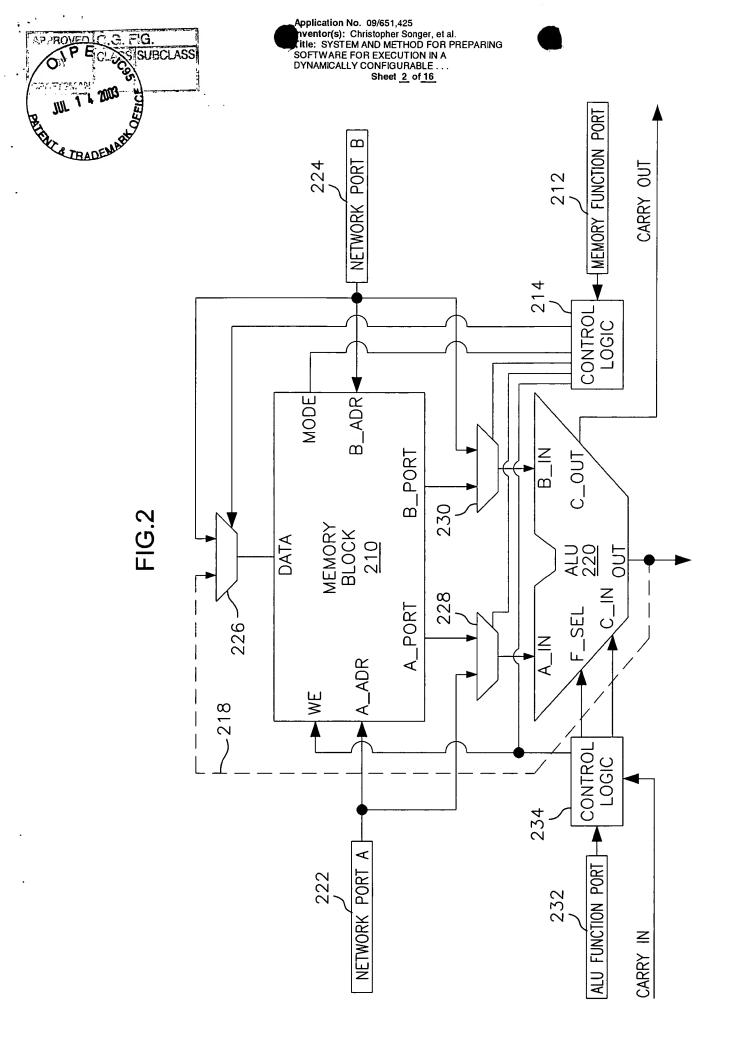
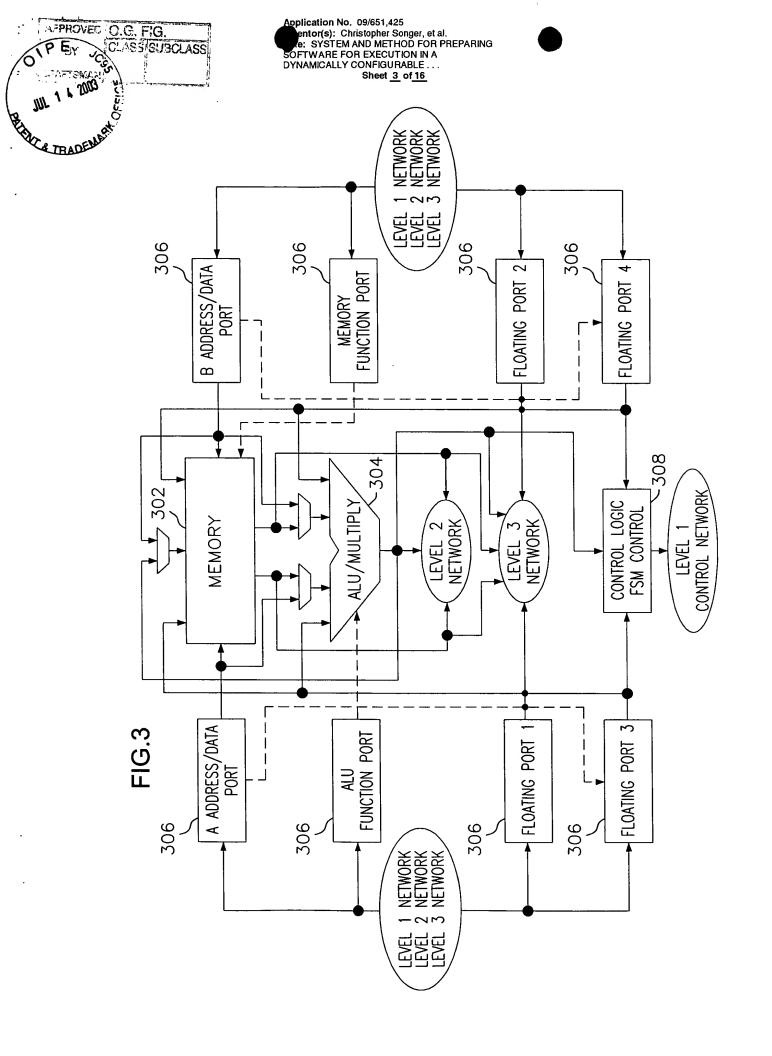
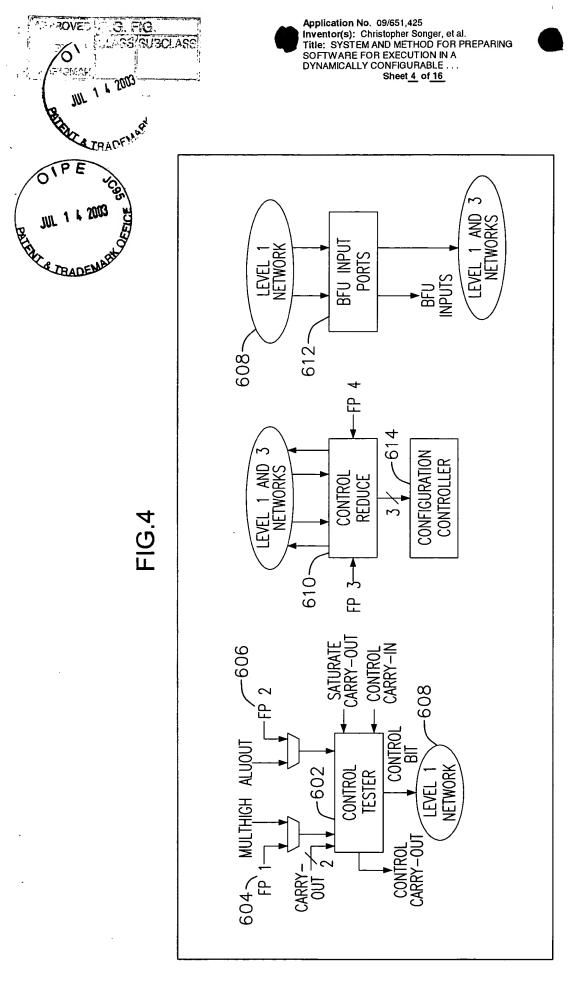
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I/0 PORT 1/0 Port 1/0 PORT 1/0 PORT 1/0 PORT CONFIGURABLE INSTRUCTION DECODER **PROGRAMMING** CONTROLLER 106 102 110 1/0 PORT 1/0 PORT CONFIGURABLE MEMORY ARRAY 1/0 Port 1/0 Port 1/0 PORT 1/0 PORT 1/0 PORT NO PORT M 1/0 PORT 1/0 PORT 110 1/0 Pórt 1/0 PORT 1/0 Port 1/0 Port 1/0 PORT 110. 104

FIG.1



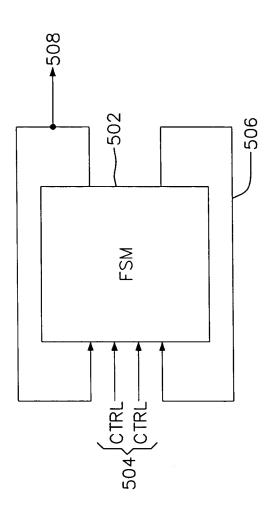






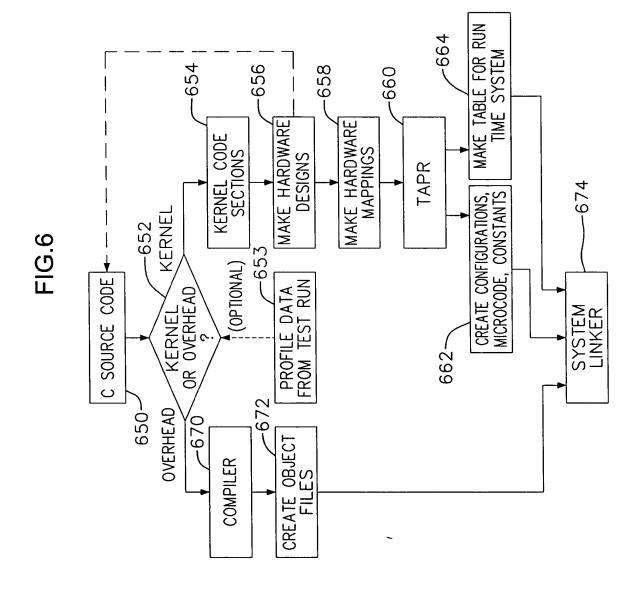
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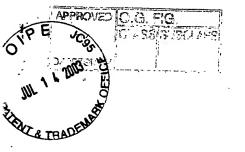
FIG.5



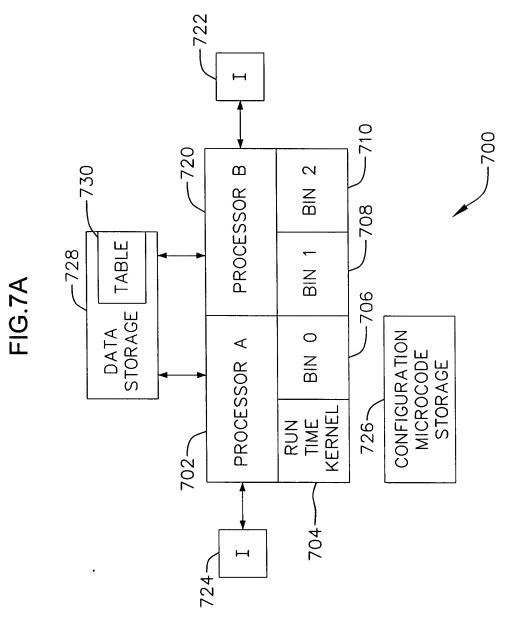


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Inventor(s): Christopher Songer, et al.
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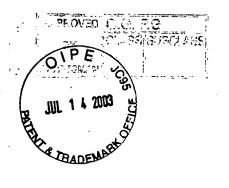
Application No. 09/651,425
Inventor(s): Christopher Songer, et al.
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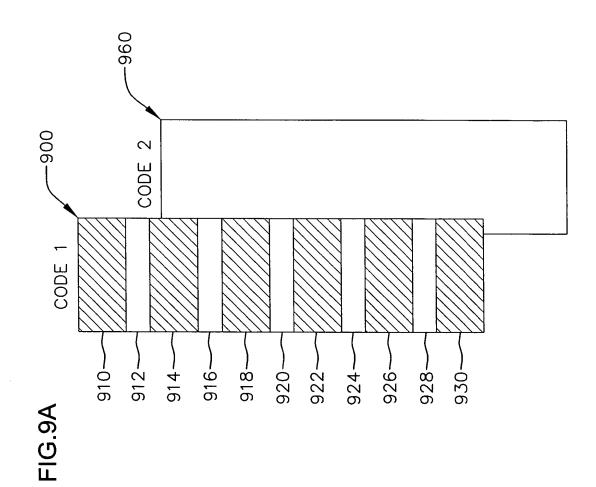
760 2 780 $\mathbf{\omega}$ DSP PROCESSOR 758 TABLE 778 DSP FIG.7B 756 DATA STORAGE 0 PROCESSOR A DSP KERNEL RUN TIME 752-754

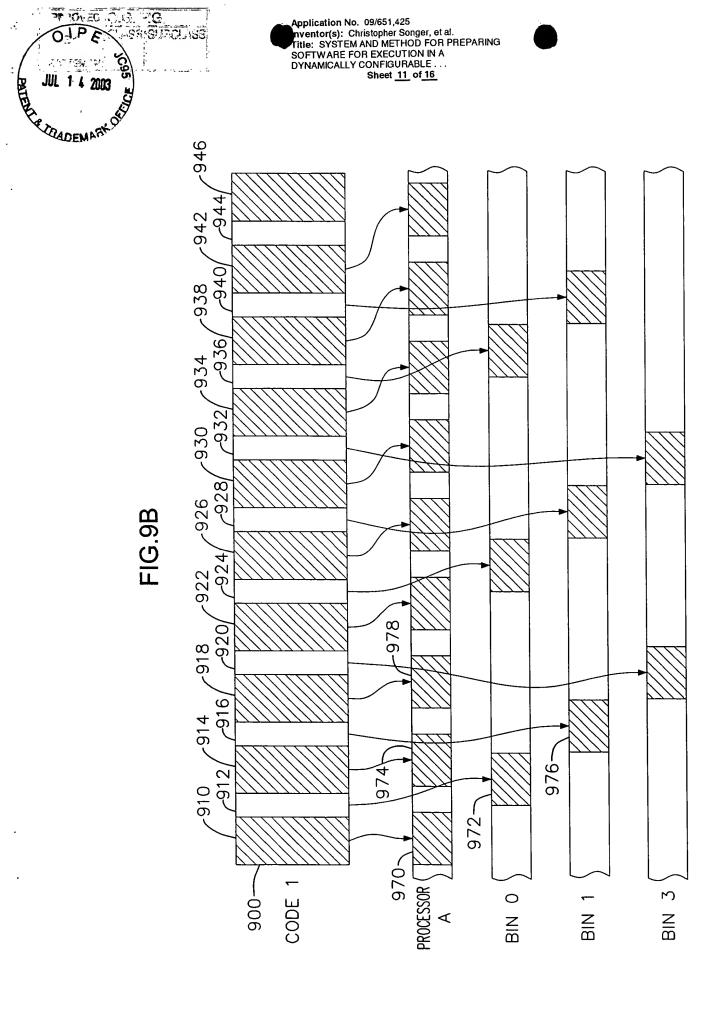
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F<u>IG.8</u>

	CONFIGURATION DMA	802
	MICROCODE DMA	-804
RTK	ARGUMENTS DMA	908
	RESULTS DMA	808
	CONFIGURATION NETWORK SOURCE	810
• PERFORMS • PERFORMS • PERFORMS	PERFORMS BACKGROUND LOADING PERFORMS COMPLETION DETECTION PERFORMS COORDINATION	NO ON







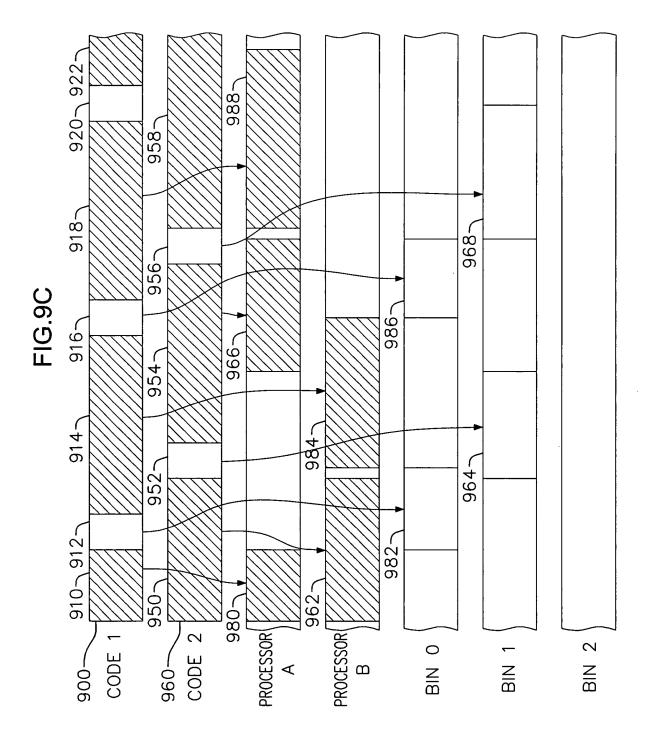


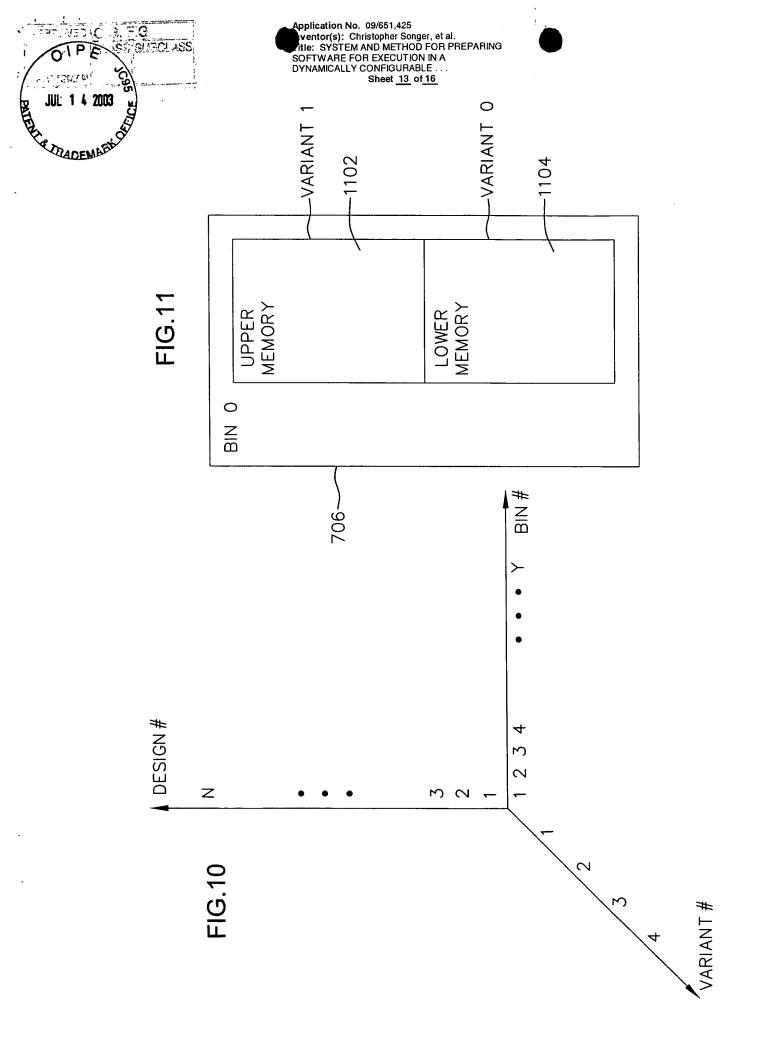
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BIN 0 BIN 1 BIN 2 MEMORY 710 1212 MEMORY 1204

FIG. 12

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FIG.13

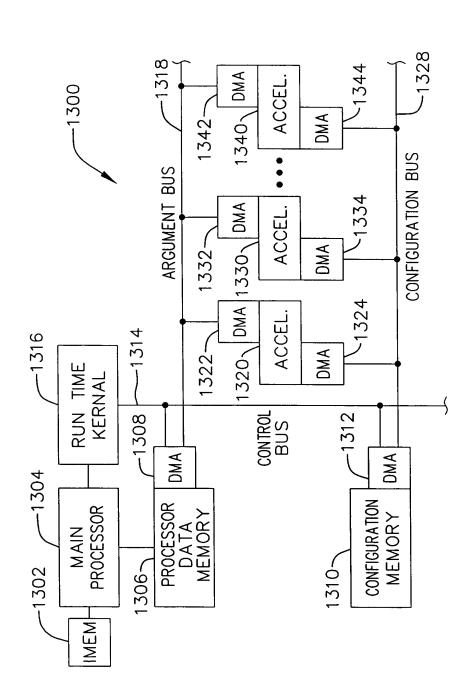
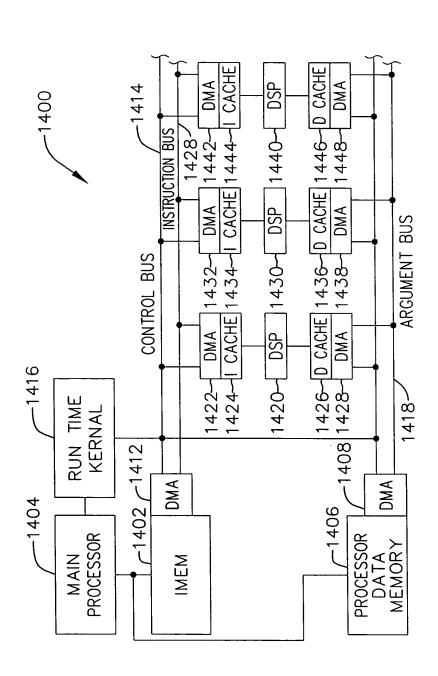


FIG.14



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